30.1 40Gb/s High-Gain Distributed Amplifiers with Cascaded Gain Stages in 0.18μm CMOS

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High-gain distributed amplifiers (DAs) are implemented in a standard 0.18μm CMOS process. By using cascaded gain stages as the distributed cells, the gain, bandwidth, and output power of the amplifiers can be increased simultaneously while maintaining input and output impedance matching. Based on the proposed architecture, 2 DAs are fabricated for demonstration. Implemented in a CMOS technology with a cut-off frequency of 50GHz, a GBW of up to 394GHz is achieved.

By incorporating the capacitance from the active devices into the input and output synthetic transmission lines, the bandwidth limitations of the DAs are thus alleviated. With recent advances in deep submicron technologies, CMOS DAs with a bandwidth up to tens of GHz have been reported [1-5]. However, the gain of these amplifiers is typically limited by the inherently low transconductance of the active devices and the nature of the additive gain mechanism. A 2-dimensional matrix amplifier [6] was proposed to boost the gain with the multiplicative gain mechanism. However, the maximum achievable GBW is compromised by the excessive loading on the central line. To overcome this limitation, DAs with cascaded gain stages as the distributed cells are presented in this paper. Figure 30.1.1 shows the simplified circuit schematic of the proposed DA architecture with an N×M configuration, where N gain cells are distributed along the artificial transmission lines and each gain cell is composed of M cascaded gain stages. Based on the small-signal equivalent circuit shown in Fig. 30.1.2, the voltage gain of the proposed circuit is derived as $ng_m{}^M Z_L{}^{(M-1)}Z_0/2$, where n is the number of distributed elements along the input/output transmission line, g_m is the transconductance of each single gain stage, Z_L is the inter-stage impedance, and Z_0 is the equivalent characteristic impedance of the drain line. Compared with conventional N-stage DAs, the gain is enhanced by a factor of $(g_m Z_L)^{M-1}$. Furthermore, since the output transmission line is loaded by the last cascaded stages of the gain cells, high output power can be achieved in contrast to cascaded single-stage distributed amplifiers (CSSDAs) [5].

Two DAs are implemented in this work. The first one is in a 3×3 configuration for high output power while the second one is designed based on a 2×4 configuration for maximum GBW. Figure 30.1.3 shows the schematic with the on-chip components for a representative N×M distributed amplifier. The input and output synthetic lines are realized by a coplanar waveguide (CPW) structure to minimize the substrate losses at higher frequencies, and 50Ω resistors in series with large bypass capacitors (C_{p1} and C_{p2}) are utilized as the termination to prevent gain roll-up at low frequencies. For an enhanced gain, identical cells are distributed along the synthetic lines, each having amplifier stages in cascade. In consideration of the stability, maximum available gain and output-to-input isolation, cascode amplifiers are used as cascaded stages. For the proposed DA architecture, loading transistors with a reduced size are used to achieve a high cut-off frequency of the input and output transmission lines, which is 60GHz in this design. Consequently, the bandwidth is limited by the design of the gain cells with cascaded amplifier stages. To alleviate the bandwidth limitations, series and shunt inductances (L_p and L_s) are used to form multiple resonances with the input capacitance of the succeeding stages [7]. In addition, inter-stage matching inductors L_i are inserted between the common-source and the common-gate transistors to maintain pass-band gain flatness. Note that cascading amplifier stages may result in undesirable peaking in the frequency response of the gain cells. The staggering technique [8] is adopted in the design of the inter-stage matching. Due to the use of the identical transistor sizes, the gain peaking of the individual gain stages is shifted in a predetermined way as the values of L_i are down-scaled along the signal traveling paths. With a proper down-scaling factor, 1.3 in this particular design, of the staggering stages, a flat gain response of the DA can be achieved. In consideration of the required circuit performance, the line width and spacing of the CPW are 6 and 20μm, respectively, leading to an unloaded characteristic impedance of 80Ω. On the other hand, spiral inductors are used to implement the peaking inductors for a compact circuit layout. Based on full-wave EM simulations, the Q-factors of the CPW and the inductors are generally higher than 10 for a frequency up to 40 GHz.

The proposed DAs are implemented in a standard 0.18μm CMOS process. On-wafer probing is used to characterize the circuit performance. Figure 30.1.4 shows the measured S-parameter from 0.1 to 40GHz., The 3×3 DA achieves a pass-band gain of 16.2dB with ±1.0 dB gain variation and a 3dB bandwidth of 33.4GHz while consuming a DC power of 260mW from a 2.8V supply. With a power consumption of 250mW, the 2×4 DA exhibits a 20dB gain and a 3dB bandwidth of 39.4GHz. The input and output return losses of the DAs are generally better than 10dB within the entire frequency band. By sweeping the input power level at various frequencies, the gain compression measurement is performed to evaluate the linearity of the amplifier. The measured output P_{1dB} of the 2×4 DA is 6.5dBm at 20GHz. With more gain cells in the distributed architecture, the 3×3 DA demonstrates a P_{1dB} of 8.4dBm at the same frequency. With a 2^7-1 PRBS at 40Gb/s, the measured eye-diagrams are illustrated in Fig. 30.1.5. Note that the input amplitude of the 2×4 DA is halved to prevent output saturation. The performance summary of the fabricated DAs along with results from the state-of-the-art CMOS DAs are presented in Fig. 30.1.6. Fig. 30.1.7 shows the die micrographs.

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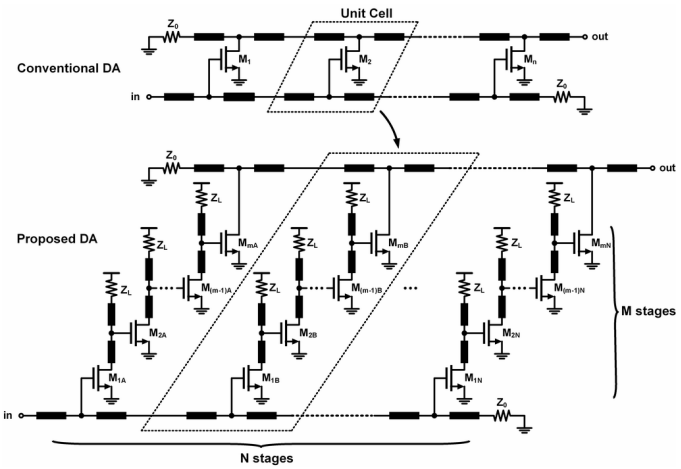

Figure 30.1.1: The proposed N×M distributed amplifier.

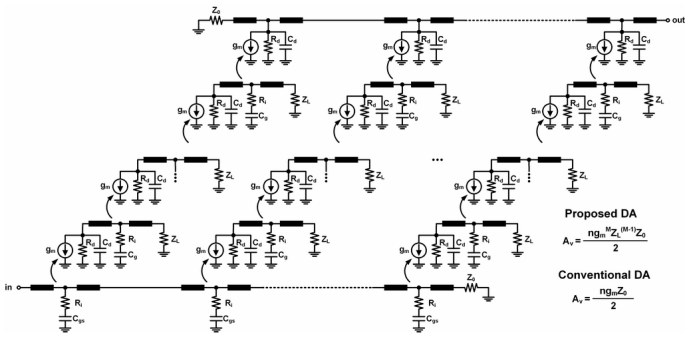

Figure 30.1.2: Small-signal equivalent circuit of the DA.

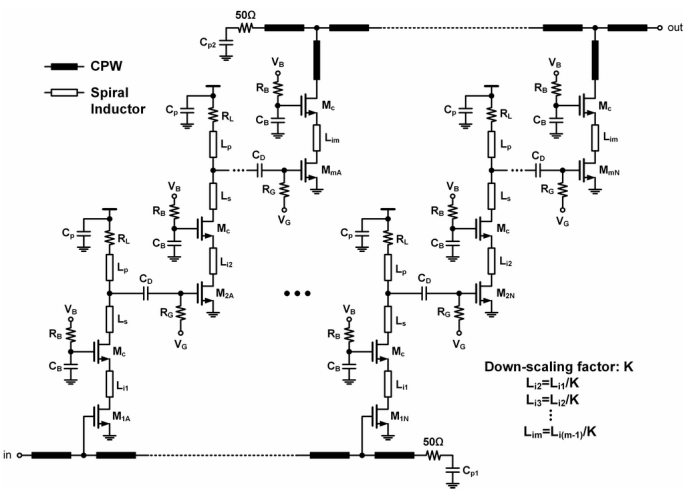

Figure 30.1.3: Circuit schematic of the DA with a N×M configuration.

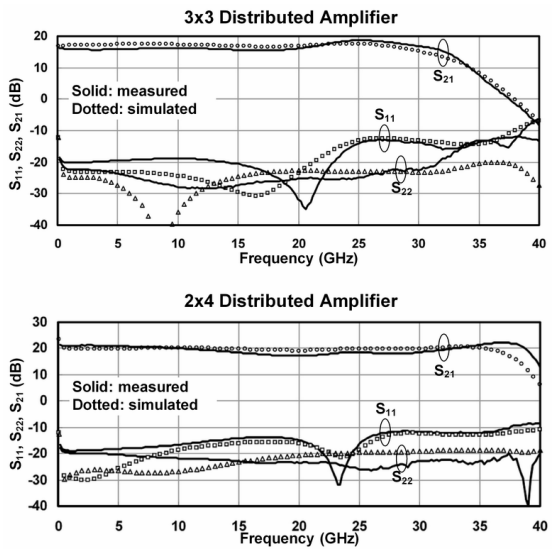

Figure 30.1.4: Measured S-parameters of the fabricated DAs.

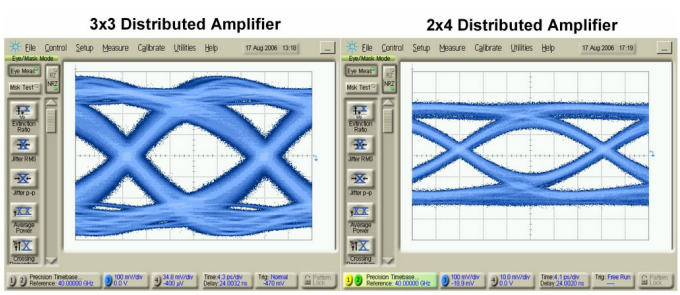

Figure 30.1.5: Measured eye-diagrams of the fabricated DAs.

Ref.	Technology	S_{21} (dB)	S_{11}/S_{22} (dB)	BW (GHz)	GBP (GHz)	P_{1dB} (dBm)	P_{diss} (mW)	Area (mm^2)
[1]	0.18μm CMOS	7.3	<-8/<-9	22	56	-	52	1.35
[2]	0.18μm CMOS	4.0	<-10/<-10	39	70	-	140	3.3
[3]	0.12μm SOI	11	<-7/<-5	90	320	12	210	1.28
[4]	90nm CMOS	7.4	<-10/<-8	80	190	-	120	0.72
[5]	90nm CMOS	7	<-7/<-12	70	157	10	122	0.72
[6]	0.18μm CMOS	9.5	<-10/<-12	50	150	7	420	1.54
This (3x3-DA)	0.18μm CMOS	16.2	<-11/<-12	33.4	216	8.4	260	2.3
This (2x4-DA)	0.18μm CMOS	20.0	<-10/<-20	39.4	394	6.5	250	2.24

Figure 30.1.6: Performance summary and comparison.

Continued on Page 620

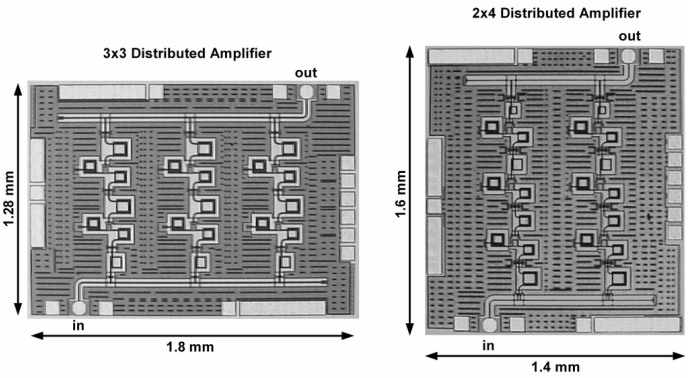

Figure 30.1.7: Micrographs of the fabricated DAs.

